Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **BASE Q1**
2. **EMMITTER Q1**
3. **COLLECTOR Q1**
4. **EMITTER Q2**
5. **BASE Q2**
6. **COLLCEOTR Q2**
7. **EMITTER Q3**
8. **BASE Q3**
9. **COLLECTOR Q3**
10. **EMITTER Q4**
11. **BASE Q4**
12. **COLLECTOR Q4**
13. **EMITTER Q5**
14. **BASE Q5**
15. **COLLECTOR Q5**
16. **N/C**

**2 1 16 15**

**14**

**13**

**12**

**11**

**7 8 9 10**

**3**

**4**

**5**

**6**

**MASK**

**REF**

**DIE ID**

**50367A**

**HFA-3096**

**50367A1**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: 50367A**

**APPROVED BY: DK DIE SIZE .052” X .053” DATE: 8/25/21**

**MFG: INTERSIL THICKNESS .015” P/N: HFA3096**

**DG 10.1.2**

#### Rev B, 7/1